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PATENT NUMBER and  
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U.S. UTILITY Patent Application

A N A N	APPL NUM 10047013	FILING DATE 01/16/2002	CLASS 257	SUBCLASS -	GAU 2811	EXAMINER Erden
**APPLICANTS: Rosner Wolfgang; Schulz Thomas; Risch Lothar; Augle Thomas; Schafer Herbert; Franosch Martin;						
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A CON OF PCT/DE00/02316 07/17/2000						
** FOREIGN APPLICATIONS VERIFIED: GERMANY 199 33 564.8 07/16/1999						
PG-PUB	DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed 35 USC 119 conditions met Verified and Acknowledged Examiner's initials			<input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO L&L-I0232	
TITLE : Method for producing a vertical semiconductor transistor component and vertical semiconductor transistor component						
U.S. DEPT. OF COMM./PAT & TM-PTO-435L(Rev. 12-94)						

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING		
Amount Due	Date Paid	Sheets Drwg. Figs.Drwg. Print Fig.		
Primary Examiner				
TERMINAL DISCLAIMER		Application Examiner		
PREPARED FOR ISSUE				
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